Supreme Court, U.S.
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No. _____

IN THE
SUPREME COURT OF THE UNITED STATES

JAMES CONSTANT

Petitioner,

v.

COMMISSIONER OF PATENTS AND TRADEMARKS

Respondent.

On Petition For Writ Of Certiorari To The United States Court Of Appeals For The Federal Circuit

---

PETITION FOR WRIT OF CERTIORARI

James Constant
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Pro-per Petitioner

4/9pp

QUESTIONS PRESENTED FOR REVIEW

Did the Federal Circuit review the Patent Office decision impermissibly under the "clearly erroneous" standard of Federal Rule of Civil Procedure 52(a) and thus nullify the "substantial evidence" standard required by 5 USC 706?

Does the "substantial evidence" standard of 5 USC 706 dictate a different outcome of judgment than does the "clearly erroneous" standard of Federal Rule of Civil Procedure 52(a)?

Is the "clearly erroneous" standard of Federal Rule of Civil Procedure 52(a) so vaguely defined making its use inherently arbitrary?

Does the judiciary share with Congress the power to make the "clearly erroneous" standard of Federal Rule of Civil Procedure 52(a)?

Is the "clearly erroneous" standard of Federal Rule of Civil Procedure 52(a) necessary and proper for carrying into execution the power to promote the progress of science?

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PETITION FOR WRIT OF CERTIORARI TO THE UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

Petitioner, James Constant, respectfully prays that a writ of certiorari issue to review the decision of the United States Court of Appeals for the Federal Circuit entered on 5/10/01 affirming the decision of the United States Patent and Trademark Office (PTO) Board of Appeals affirming an examiner's rejection of all the pending claims in the petitioner's patent application as being obvious under 35 USC 103, over a single cited prior art reference cited in an earlier court/court case *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988).

OPINIONS BELOW

The unpublished decision of the Federal Circuit appears in Appendix A to this Petition. The unpublished decision of the Federal Circuit denying the petitioner's Petition for a Rehearing appears in Appendix B to this Petition. The unpublished Decision of Board of Patent Appeals affirming the Examiner's decision of obviousness appears in

Appendix C to this petition. The unpublished Decision of the Board of Patent Appeals granting petitioner's Request for Rehearing but denying the request to make any changes in its decision of obviousness appears in Appendix D to this petition.

JURISDICTION

The Court of Appeals decision was entered on 5/10/01 and its decision denying petitioner's Petition for a Rehearing was entered on 6/1/01. This Court's jurisdiction is invoked under Title 28 USC 1254(1).

STATUTORY PROVISIONS INVOLVED

The provisions of Constitution Art. 1, Sec. 8, Cl. 8 and last paragraph, statutes 5 USC 706 and 35 USC 103, and Federal Rule of Civil Procedure 52(a) are set forth in the petition.

STATEMENT OF THE CASE

Petitioner applied for a patent for a single chip digital semiconductor signal processor. The PTO patent examiner concluded that the petitioner's apparatus was obvious in light of prior art and denied the application. 35 USC 103. The PTO's review board (The Board of Patent Appeals and Interferences) upheld the examiner's decision. The petitioner sought review in the Federal Circuit,

where a panel treated the question as one of res judicata of facts and law already decided in the earlier case *Constant, supra* under the court/court "clearly erroneous" standard of FRCP 52(a) and falsely held that "we review the Board's underlying factual findings for substantial evidence". Appendix A.

REASONS FOR GRANTING THE WRIT

This Court has stressed the importance of not simply rubber-stamping agency fact-finding. The Administrative Procedure Act (APA) requires meaningful review; and its enactment meant stricter judicial review of agency fact-finding than Congress believed some courts had previously conducted. *Dickinson v. Zurko*, 119 Sct 1816 (1999) at III. citing *Universal Camera,* 340 U.S. at 490.

A. STANDARDS OF REVIEW

The APA sets forth standards governing judicial review of findings of fact made by the Patent and Trademark Office (PTO). 5 USC 706. The Federal Circuit must use the framework set forth in that section. Section 706 says that a

> "**reviewing court shall** . . . (2) hold unlawful and set aside agency . . . findings . . . found to be . . . (A) arbitrary, capricious, [or] an abuse of discretion,

> or . . .(E) unsupported by substantial evidence in a case subject to sections 556 or 557 of this title or otherwise reviewed on the record of an agency hearing provided by statute . . . In making the foregoing determinations, **the court shall review the whole record or those parts of it cited by a party** . . ." Bold emphasis added.

Thus, findings which are arbitrary, capricious, in abuse of discretion, and unsupported by substantial evidence are expressly prohibited by the Section 706 standard of review.

On the other hand, the "clearly erroneous" standard of Rule 52(a) states that

> (a) . . . Findings of fact shall not be set aside unless clearly erroneous . . .

Federal Circuit Practice

The Federal Circuit is addicted to its practice under Rule 52(a) and it is hard to kick its habit even after this Court held that "the federal Circuit must use the framework set forth in that section [5 USC 706]". *Zurko, supra* 1st paragraph. This is all evident in the present case in which the Federal Circuit did not examine all the facts prescribed by this Court in

Graham v. John Deere Co., 383 U.S. 1, 17-18, 86 S. Ct. 684, 694, 15 L. Ed. 2d 545 (1966) but, rather, held that the only fact of consequence which obviates the invention is the Springer reference cited in the earlier case *Constant*, *supra* decided under Rule 52(a). See Appendix A page 3 next to last paragraph.[1] Such "review" flies in the face of 5 USC 706 which requires that, in making determinations, "the court shall review the whole record or those parts of the record cited by a party". As demonstrated in the present case, the Federal Circuit believes that there is no practical difference between the "clearly erroneous" standard of Rule 52(a) and the "substantial evidence" standard of 5 USC 706.

Differences Between Standards

The practical difference in outcome depends upon which standard is used although, apart from the *Zurko* case, this Court has failed to uncover a single instance in which a reviewing court conceded that use of one standard rather than the other would in fact have produced a different outcome. *Zurko, supra* at III. However, one has only to look at how courts make their decisions under each standard. While the "substantial evidence" standard is objec-

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[1] Nor did the PTO examine all the facts prescribed by this Court in *Graham, supra* but, rather, without any suggestion of the invention improved elements in the prior art, relied solely on the artisan's high skill to obviate the invention. See Appendices C and D.

tive and counts facts the "clearly erroneous" standard is subjective and leaves it up to the judge to chose and say what the facts and law are. The essence about the clearly erroneous standard is that it is so vaguely defined, making its use inherently arbitrary. Judges like it because it lets them chose and say what the facts and law are. In patent cases it permits them to say what the facts and law are and thus, through summary judgment, to forego jury trials and to easily obviate patents and dispose proceedings without considering facts and law of patent infringement and, in appeals, without the burden of "review of the whole record or those parts of it cited by a party" prescribed by 5 USC 706. In contrast, the Section 706 court/agency standard removes a judge's discretion from saying what the facts and law are.

For example, in *Constant, supra*, on motion for summary judgment by corporate infringers, petitioner's two patents were found invalid and sanctions were imposed, *without hearing petitioner's facts and claims of patent infringement and without the requested jury trial.* Review by the Federal Circuit was made under the clearly erroneous standard using the judge's choice of facts and law of patent validity and overlooking the petitioner's facts and law of patent infringement. However, a court's jurisdiction rests on the patent owner's claim of patent infringement and not on the alleged corporate infringer's claim of patent invalidity. *Christianson v.*

Colt Industries (1988) 108 SCT 2166, 100 LEd2d 811.

Federal Circuit Nullifies 5 USC 706

In the *Zurko* case, *supra*, this Court held that the Federal Circuit review of PTO findings of fact must use the substantial evidence standard of 5 USC 706 without any exception. Since the Federal Circuit traditionally has used the clearly erroneous standard of Rule 52(a), all cases reviewed by that court are legally tainted, a fact not gone unnoticed by the PTO which brought the *Zurko* case to reinstate the substantial evidence standard. However, the nullification of 5 USC 706 in court/agency cases continues and the use of the Rule 52(a) standard in court/court cases is an anomaly between standards which this Court has not addressed.

In the present case the Federal Circuit refused to review the Graham factors and thus failed to "review the whole record or those parts of it cited by a party", as required by 5 USC 706. See the Federal Circuit decisions in the Appendix Parts A and B. Instead, the Federal Circuit applied res judicata based on the case *Constant, supra* involving different parties, different inventions, different issues, different claims and decided under the clearly erroneous standard. Thus, having foregone the consideration of objective substantial evidence under each part of the Graham factors, the Federal Circuit has,

in effect, nullified the court/agency rule standard of 5 USC 706. Under such nullification, the court/agency "substantial evidence" standard of 5 USC 706 and the obviousness standard 35 USC 103 both suspend leaving the Federal Circuit to decide all cases the impermissible but easy way under Rule 52(a) with knowledge that the chance of review by this Court is almost null.[2] For all practical purposes, the *Zurko*, *supra* decision by this Court does not exist and Rule 52(a) is, in effect, the practical standard of review in the Federal Circuit.

Anomalous Rule 52(a)

The petitioner believes the Rule 52(a) standard is a vaguely defined judge-made and, therefore, unconstitutional standard making its use by judges inherently arbitrary. This is evident when comparing the text of subjective Rule 52(a) (made by the judiciary) to the text of objective Section 706 (made by Congress).

The Federal Rules of Civil Procedure are proposed by the Judicial Conference and this Court submits them to Congress for its approval which, for the most part, is almost automatic. While some of these rules are necessary for housekeeping purposes, Rule

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[2] Since 1982, this Court has granted certiorari in only 31 appeals heard in the Federal Circuit. Almost 1,000 petitions for certiorari have been filed in that period.

52(a) usurps the Congressional power to secure inventor's rights. It gives the judiciary the power to arbitrarily say what the facts and law are in *Constant, supra* and in the present case. The anomaly of Rule 52(a) in court/court cases should be recognized and addressed by this Court as it already has been recognized and addressed by the PTO and this Court in the court/agency case *Zurko, supra.*

The last paragraph of Article 1 Section 8 of the Constitution gives the legislature the exclusive power

> To make all laws which shall be necessary and proper for carrying into execution the foregoing powers . . .

including the Article 1 Section 8 Clause 8 power

> To promote the progress of science and the useful arts, by securing for limited times to authors and inventors the exclusive right to their respective writings and discoveries.

The petitioner finds nothing in the Constitution that calls for the judicial sharing of the congressional exclusive power "to make all laws ...". Moreover, if the Section 706 standard is deemed "necessary and proper for carrying into execution . . ." the power "to promote the progress of science . . ." the Rule 52(a) standard falls short of the Section 706

standard. Rule 52(a) is unconstitutional because it is proposed by the judiciary, not by Congress, and because it falls short of being "necessary and proper for carrying into execution . . ." the power "to promote the progress of science . . .".

B. DIFFERENT OUTCOME DICTATED BY SUBSTANTIAL EVIDENCE STANDARD

Evidence Considered

The sole evidence considered by the Federal Circuit is what it subjectively and arbitrarily says is the evidence, namely, the Springer reference cited in the *Constant* case, *supra*. The Federal Circuit relies on this earlier case which held that Springer "suggested using RAMs in place of shift registers" and "Constant's own admission that the Springer reference taught him to substitute RAMs for shift registers". This is not Section 706 objective substantial evidence obtained from consideration of all Graham factors but subjective evidence based on a single reference of what judges say the evidence is under the clearly erroneous standard. Moreover, the Federal Circuit's decision is wrong and uncritical on merits (1) wrong because res judicata is based on the earlier court/court case *Constant, supra* with different parties, different inventions, different issues, different claims, different prior art (except for the Springer reference used to obviate the present inven-

tion), and different standard of review and (2) uncritical because these holdings mischaracterize what exactly is suggested by the Springer reference and what Constant admits. More accurately, Springer *teaches* using RAMS *to produce a serial access shift register on 4 digital semiconductor chips.* Had the petitioner used Springer's *teaching* the claimed invention would use RAMS *to produce a serial access shift register on 4 digital semiconductor chips.*

Evidence Overlooked

The putting of RAM and associated circuits on semiconductor chips is disclosed in the specification and parent patent 3,950,636. The Springer reference ('635 patent col 4 lines 19-24) shows RAMs and associated circuits on multiple digital semiconductor chips, and references to SN 7489, AM27503, 310IT, uA9103, and NA7599 ('635 patent col 4 lines 47-50) each shows RAM and associated circuits on single digital semiconductor chips. The putting of non-RAM circuits on digital semiconductor chips is also disclosed. The Buie and Brewer reference shows a shift register and associated circuits on a single digital semiconductor chip, and such devices can be assembled from conventional medium scale integrated circuit logic (MSI) or can be designed in large scale integrated (LSI) form ('635 patent col 2 lines 3-10). The issue, therefore, is not whether RAMs can

be placed on single or multiple chips. This is done by the Springer, SN 7489, AM27503, 310IT, uA9103, and NA7599 RAMs disclosed in the specification. Rather, the issue is whether the claimed invention which incorporates RAM, not the claimed RAM means, can be placed on single or multiple chips. This evidence was overlooked by the Federal Circuit.

Graham Factors Overlooked

The obviousness standard of 35 USC 103 states that:

> A patent may not be obtained . . . If the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The ultimate determination of whether an invention is obvious or not at the time it was made is a legal conclusion based on the following factual inquiries: the scope and content of the prior art; the level of ordinary skill in the prior art; the differences between the claimed invention and the prior art; and

objective secondary considerations. *Graham, supra.*

Had the Federal Circuit and PTO considered the Graham factors under the substantial evidence standard, it would have found them [with reference to petitioner's Brief (App.Br.), Reply (App.R.), and Appendix (Appx.) in the Federal Circuit] as follows: The **scope and content of the prior art** are means for signal processors such as the Swan patent (which describes an analog delay line signal processor) and the uncited Whitehouse, Byram, and Buie and Brewer articles which describe a signal processor as a shift register placed on a single chip digital semiconductor. App.Br. 11-12 (Whitehouse Fig 14); Appx. (Prior Art Cited In Application and Parent Patent). The Springer reference describes a serial access shift register implemented with 4 digital semiconductor RAM (random access memory) chips. Regarding the **level of ordinary skill in the prior art**, while high it does not exceed the level of skill of acknowledged U.S. and NATO experts Whitehouse, Byram, and Buie and Brewer who implement a digital signal processor on a single chip but fail to suggest use of a RAM. The skilled person cannot do what the acknowledged real world experts failed to do. The **differences between the claimed invention and the prior art** are between the invention's single chip digital semiconductor signal processor implemented with RAM and the prior art which does not suggest placing a digital signal processor with RAM on a single semiconductor chip.

The **secondary considerations** are that the references do not suggest the problem and solution provided by the invention which the specification discloses in detail, that the references cannot be combined, that the references teach away from the invention, and the presence of a commercial response. App.Br. 19-31; App.R.2. Although objective considerations are labeled "secondary", evidence of such considerations must be evaluated prior to reaching a conclusion on a patented item's obviousness; indeed, such evidence alone may often establish an invention's nonobviousness. *Demaco Corp. v. F. Von Langsdorff Licensing Ltd.*, 851 F.2d 1387, 1391 (Fed. Cir. 1988). Likewise, the commercial response to an invention is also a significant factor in evaluating obviousness since it provides objective evidence of how the patented device is viewed in the marketplace by those directly interested in the product; indeed, commercial success is often a harbinger of nonobviousness and may establish that an invention appearing to have been obvious was in fact not obvious. *Arkie Lures, Inc. v. Gene Larew Tackle, Inc.*, 119 F.3d 953, 957 (Fed. Cir. 1997); *Demaco,* 851 F.2d at 1391. When a patentee asserts that commercial success supports its contention of nonobviousness, there must be a sufficient nexus between the commercial success and the patented invention. *Demaco,* 851 F.2d at 1391. The requisite nexus may be demonstrated by merely showing that there is commercial success and that the product that is commercially

successful is the patented invention. The record of the earlier decision *Constant, supra* includes examples of single chip digital semiconductor signal processors implemented with RAM (single chip devices manufactured by corporate defendants).

Legal Conclusions Under 5 USC 706

The PTO failed to make each test and failed to consider the prior art as a whole, namely, the Whitehouse, Byram, and Buie and Brewer references. The PTO used the less relevant Swan and Springer combination instead of the more relevant Whitehouse, Byram, and Buie and Brewer references. The latter references are more relevant than the former references because they represent the state of art of digital single chip signal processors made by acknowledged real world U.S. and NATO experts at the time the invention was made.

The PTO impermissibly invokes the high level of skill in the art to provide motivation to combine references. A lofty level of skill alone does not suffice to supply a motivation to combine. *In re Rouffet* (CAFC) 7/15/98 No. 97-1492. To imbue one of ordinary skill in the art with knowledge of the invention in suit, when no prior art reference or references of record convey or suggest that knowledge, is to fall victim to the insidious effect of a hindsight syndrome wherein that which only the inventor taught is used

against its teacher. *W. L. Gore & Assocs., Inc. V. Garlock, Inc.*, 721 F2d 1540,1553, 220 USPQ 303,312-313 (CAFC 1983).

Since the prior art does not suggest a single chip digital semiconductor signal processor implemented with RAM, the PTO's conclusions of law are based solely on the skill of the artisan and thus on conjectures not facts. "If the prior art does not show or suggest the improved element itself, it defies logical reasoning to say that the same prior art suggests the use of that improved element in a combination". *In re Bernhart*, 417 F2d 1395, 163 UPS 618 (CCPA 1969). Accord: *Radio Steel & Mfg Co. v. MTD Products, Inc.*, 731 F2d 840, 221 UPS 657 (CAFC 1984), *cert. den.* 469 US 831 (1984). App.Br.17. The Federal Circuit claims that it upholds the PTO's fact findings unless they are unsupported by substantial evidence in the record. *In re Hyatt*, 211 F3d 1367,1372, 54 USPQ2d 1664, 1667 (CAFC 2000).

Objections Overlooked

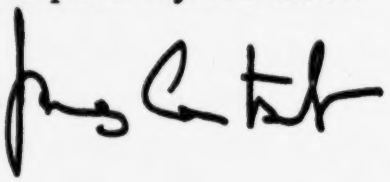
The petitioner objected to the decision in *Constant, supra* on grounds it was obtained without jurisdiction and through mischaracterization of the Springer reference. App.Br. 2, App.R. 3-5. The petitioner also objected to the patentability statutes used to obviate the '635 patent in *Constant, supra* on grounds these statutes are unconstitutional in civil

(but not PTO) actions under the Constitutional Enabling Provision Art 1, Sec 8, Cl 8. These objections challenge the validity of the earlier case *Constant, supra* on grounds of jurisdiction and constitutional validity. They were denied by the Federal Circuit's decision on rehearing.

CONCLUSIONS

For the reasons set forth above, a writ of certiorari should issue to review the decision of the Federal Circuit in this matter.[3] The denial of this petition will, in effect, give the Federal Circuit the green light to continue its nullification of the substantial evidence standard of 5 USC 706 and continue its practice of using the clearly erroneous standard of Rule 52(a) as the standard of review.

Respectfully submitted



Dated: 30 August, 2001

James Constant
Pro Per Petitioner

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[3]If this Court elects not to address the issues presented in this writ at the present time, it is requested that the writ issue and that the matter be remanded to the Federal Circuit for appropriate findings and conclusions.

NOTE: Pursuant to Fed. Cir. R. 47.6, this disposition is not citable as precedent. It is a public record. This disposition will appear in tables published periodically.

United States Court of Appeals for the Federal Circuit

01-1125
(Serial no. 08/210,241)

IN RE JAMES N. CONSTANT

DECIDED: May 10, 2001

Before MAYER, Chief Judge, LINN and DYK, Circuit Judges. PER CURIAM.

James Constant appeals a final decision of the United States Patent and Trademark Office Board of Patent Appeals and Interferences ("Board") affirming an examiner's rejection of all of the pending claims in Constant's patent application as being obvious, under 35 U.S.C. § 103(a), over the cited prior art. Ex Parte Constant, Paper No. 23 (B.P.A.I. Oct. 19, 2000) (denying request for rehearing); Ex Parte Constant, Paper No. 21 (B.P.A.I. Aug. 18, 2000) (affirming rejection).

The ultimate determination of whether an invention would have been obvious under 35 U.S.C. § 103(a) is a legal conclusion based on underlying findings of fact. In re Dembiczak, 175 F.3d 994, 998,

50 USPQ2d 1614,1616 (Fed. Cir. 1999). We review the Board's ultimate determination of obviousness de novo. Id. However, we review the Board's underlying factual findings for substantial evidence. In re Gartside, 203 F.3d 1305, 1316, 53 USPQ2d 1769, 1776 (Fed. Cir. 2000).

Constant has been a party in a number of cases that have come before this court. Constant opens his appeal with a blanket request for the recusal of any judge involved in one of his earlier cases "on grounds of judicial bias evidenced by making decisions against the appellant." Although Constant asserts that the decisions in these cases violated the Constitution and various statutes, his claim of bias is based on nothing more than a disagreement with those decisions. However, disagreement with an earlier decision does not constitute a ground for recusal in a later case. See Liteky v. United States, 510 U.S. 540, 551 (1994) ("Also not subject to deprecatory characterization as 'bias' or 'prejudice' are opinions held by judges as a result of what they learned in earlier proceedings. It has long been regarded as normal and proper for a judge to sit in the same case upon its remand, and to sit in successive trials involving the same defendant."); Id at 555 ("[J]udicial rulings [within a trial] alone almost never constitute a valid basis for a bias or partiality motion. . . . Almost invariably, they are proper grounds for appeal, not for recusal."). Constant identifies no other grounds for recusal and we find none. Accordingly, we decline

Constant's invitation to recuse without considering whether any member of this panel has heard an earlier case involving Constant.

Turning to the merits, Constant admits that the appealed claims are substantially similar to those of the parent patent (U.S. Patent No. 3,950,635, the '635 patent), differing only by the "placing of all earlier claimed circuits on multiple chips or on a single chip." Despite that admission, Constant argues that using RAM (random access memory) instead of shift registers is another point of novelty. We remind Constant, however, of one of his earlier cases in which this court affirmed the finding that the '635 patent was invalid. Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988). In that case, we stated that the Springer reference, which is also asserted in the present case, "suggested using Rams in place of shift registers," and we specifically discussed Constant's own admission that the Springer reference "taught him to substitute Rams for shift registers." Id. at 1570, 7 USPQ2d at 1063-64. The court is no more persuaded in this case than it was before and looks with disfavor on Constant's reassertion of the same failed argument of novelty of Rams in the present invention.

We have carefully considered each of Constant's remaining arguments and find no basis on which to reverse the Board. Accordingly, and for the reasons clearly articulated in the Board's opinion, the decision of the Board is affirmed.

APPENDIX B

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

01-1125
(Serial no. 08/210,241)

IN RE JAMES N. CONSTANT

ORDER

Before MAYER, Chief Judge, LINN, Circuit Judge, and DYK, Circuit Judge.

A petition for rehearing having been filed by the APPELLANT, UPON CONSIDERATION THEREOF, it is

ORDERED that the petition for rehearing be, and the same hereby is, DENIED.

The mandate of the court will issue on June 8, 2001.

FOR THE COURT,

Dated: June 1, 2001

Jan Horbaly, Clerk

cc: James N. Constant
John M. Whealan

FILED
U.S. COURT OF APPEALS FOR
THE FEDERAL CIRCUIT
JUN — 12001
JAN HORBALY, CLERK

IN RE CONSTANT, 01-1125
(PTO 08/210,241)

Note: Pursuant to Fed. Cir. R. 47.6, this order is not citable as precedent. it is a public record.

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

MAILED
AUG 18 2000
PAT. & TM. OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JAMES N. CONSTANT

Appeal No. 1997-0239
Application No. 08/210,241

ON BRIEF

Before HAIRSTON, KRASS, and RUGGIERO, Administrative Patent Judges.
RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 1-12, 14-27, and 40, all of the claims pending in the present application. Claims 13, 28-39, and 41 have been canceled.

The disclosed invention relates to time compression and expansion in which a random access memory (RAM) , addressed sequentially by a counter, performs the function of a delay line.

Claim 1 is illustrative of the invention and reads as follows:

> 1. Digital semiconductor means for signal processing including:
>
> first random access memory means having storage locations of a predetermined number n for storing input first signals;
>
> second memory means having storage locations of a predetermined number n for storing input second signals;
>
> input means for carrying input signals into each said first and second memory means on m signal lines;

output means for carrying output signals from each said first and second memory means on m signal lines;

multiplier means for multiplying selected outputs from said first and second memory means and for providing products of multiplications;

integrator means for integrating the products of multiplications and for providing integrated products as output;

control means for operating said means for signal processing wherein said first memory means is on a first single semiconductor chip.

The Examiner relies on the following prior art references:

Swan 3,449,553 Jun. 10, 1969

John Springer (Springer), "High-speed shift registers use TTL RAMs and counters to do all the shifting," Electronic Design, pp. 146, 148 (September 1973).

Claims 1-12, 14-27, and 40 stand finally rejected as being based on an inadequate disclosure under the first paragraph of 35 U.S.C. § 112. Claims

1-12, 14-27, and 40 stand further finally rejected under 35 U.S.C. § 103 as being unpatentable over Swan in view of Springer.[1]

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the Briefs[2] and Answers for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the Examiner, the arguments in support of the rejections and the evidence of obviousness relied upon by the Examiner as support for the obviousness rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellant's arguments set forth in the Briefs along with the Examiner's rationale in support of the rejections and arguments in rebuttal set forth in the Examiner's Answers.

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[1] The Examiner's arguments additionally rely on Appellant's admissions in the specification.

[2] The Appeal Brief was filed September 16, 1994. In response to the Examiner's Answer dated December 1, 1994, a Reply Brief was filed December 12, 1994 which was acknowledged and entered by the Examiner without further comment on February 7, 1995.

It is our view, after consideration of the record before us, that Appellant's specification in this application describes the claimed invention in a manner which complies with the requirements of 35 U.S.C. § 112. We are also of the view, however, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 1-12, 14-27, and 40. Accordingly, we affirm.

We consider first the rejection of claims 1-12, 14-27, and 40 under the first paragraph of 35 U.S.C. § 112, noting that the Examiner relies on both the "written description" and "enabling" clauses of the statute. The Examiner's assertion of lack of compliance with the "written description" requirement was a result of amendments to the original disclosure and claims as detailed at pages 4 and 5 of the Answer. The function of the description requirement of the first paragraph of 35 U.S.C. § 112 is to ensure that the inventor had possession, as of the filing date of the application relied on, of the specific subject matter later claimed by him. In re Wertheim, 541 F.2d 257, 262., 191 USPQ 90, 96 (CCPA 1976)

Initially, the Examiner contends that the amendment to page 25 of the specification relating to the description of "unrestricted" multipliers lacks support in the original disclosure. We agree with

Appellants, however, that the language in question is an attempt to clarify possible ambiguities in the original disclosure by describing the differences between restricted and unrestricted multipliers. An amendment to correct an obvious error does not constitute new matter where one skilled in the art would not only recognize the existence of error in the specification, but also the appropriate correction. In re Oda, 443 F.2d 1200, 1203, 170 USPQ 268, 270 (CCPA 1971) . In our view, the skilled artisan would recognize that an exclusive-OR gate is a "restricted" multiplier in the sense that its operation is limited to particular logic operations. We further call attention to the fact that original claims 13 and 14 recite an unrestricted multiplier and a restricted exclusive-OR gate multiplier, respectively. The claims as filed in the original specification are part of the disclosure and therefore, if an application as originally filed contains a claim disclosing material not disclosed in the remainder of the specification, the applicant may amend the specification to include the claimed subject matter. In re Benno, 768 F.2d 1340, 1346, 226 USPQ 683, 686-87 (Fed. Cir. 1985)

We further agree with Appellant (Reply Brief, pages 2 and 3) that the original claims and specification provide support for the "single semiconductor chip" language of the claims before us. Original claims 1 and 2 clearly describe the implementation of memories and other circuitry on "a single semicon-

ductor chip." Original claims constitute their own description. In re Koller, 613 F.2d 819, 823, 204 USPQ 702, 706 (CCPA 1980) . Further, in our view, the description in the original specification of prior art large scale integration techniques (LSI) at page 19, lines 4-7 and page 27, lines 4-17 of the original specification, as well as the original Abstract, provide a clear description of implementation of the claimed invention on single chip circuitry. "It is not necessary that the application describe the claim limitations exactly, . . . but only so clearly that persons of ordinary skill in the art will recognize from the disclosure that appellants invented processes including those limitations." In re Wertheim, 541 F.2d at 262, 191 USPQ at 96 citing In re Smythe, 480 F.2d 1376, 1382, 178 USPQ 279, 284 (CCPA 1973). Furthermore, the Federal Circuit points out that "[i]t is not necessary that the claimed subject matter be described identically, but the disclosure originally filed must convey to those skilled in the art that applicant had invented the subject matter later claimed." In re Wilder, 736 F.2d 1516, 1520, 222 USPQ 369, 372 (Fed. Cir. 1984), cert. denied, 469 U.S. 1209 (1985), citing In re Kaslow, 707 F.2d 1366, 1375, 217 USPQ 1089, 1096 (Fed. Cir. 1983) . In our opinion, under the factual situation presented in the present case, Appellant has satisfied the statutory written description requirement because he was clearly in possession of the invention at the time of filing of the application.

Turning to a consideration of the Examiner's

35 U.S.C. § 112, first paragraph, rejection of the appealed claims for "lack of enablement," we note that, in order to comply with the enablement provision of 35 U.S.C. § 112, first paragraph, the disclosure must adequately describe the claimed invention so that the artisan could practice it without undue experimentation. In re Scarbrough, 500 F.2d 560, 566, 182 USPQ 298, 303 (CCPA 1974); In re Brandstadter, 484 F.2d 1395, 1404, 179 USPQ 286, 293 (CCPA 1973); and In re Gay, 309 F.2d 769, 774, 135 USPQ 311, 316 (CCPA 1962). If the Examiner has a reasonable basis for questioning the sufficiency of the disclosure, the burden shifts to Appellant to come forward with evidence to rebut this challenge. In re Doyle, 482 F.2d 1385, 1392, 179 USPQ 227, 232 (CCPA 1973), cert. denied, 416 U.S. 935 (1974); In re Brown, 477 F.2d 946, 950, 177 USPQ 691, 694 (CCPA 1973); and In re Ghiron, 442 F.2d 985, 992, 169 USPQ 723, 728 (CCPA 1971) . However, the burden is initially upon the Examiner to establish a reasonable basis for questioning the adequacy of the disclosure. In re Strahilevitz, 668 F.2d 1229, 1232, 212 USPQ 561, 563 (CCPA 1982); In re Angstadt, 537 F.2d 498, 504, 190 USPQ 214, 219 (CCPA 1976); and In re Armbruster, 512 F.2d 676, 677, 185 USPQ 152, 153 (CCPA 1975).

Initially, the Examiner asserts (Answer, pages 6 and 7) a lack of enabling disclosure of implementation of the claimed invention on semiconductor cir-

cuitry and, specifically, on a single semiconductor chip. The Examiner, however, has provided no evidence or line of reasoning that would establish a reasonable basis for challenging the sufficiency of the disclosure. It is our view, after reviewing the evidence of record including Appellant's description of the prior art in the specification, that the level of skill relative to large scale integration (LSI) techniques at the time of filing of Appellant's specification would enable the skilled artisan to implement the claimed invention on a single semiconductor chip without undue experimentation.

Further, on the issue of the disclosure of "unrestricted" multipliers, we find the Examiner's reliance on the "enabling" clause of the statute to be misplaced. As the Examiner admits (Answer, page 12) , unrestricted multipliers were known at the time of Appellant's invention. From the line of reasoning presented, it is apparent that the Examiner is reiterating previous arguments related to the statutory "written description" requirement. Our earlier discussion supra, however, concluded that the original disclosure including the original claims provided a clear disclosure of restricted and unrestricted multipliers including the characterization of an exclusive-OR gate as an unrestricted multiplier.

For all of the above reasons, we do not sustain the Examiner's rejection of claims 1-12, 14-27, and

40 under the first paragraph of 35 U.S.C. § 112.

We next turn to a consideration of the Examiner's 35 U.S.C. § 103 rejection of appealed claims 1-12, 14-27, and 40. As the basis for the obviousness rejection, the Examiner proposes to modify the digital correlator disclosure of Swan. In the Examiner's line of reasoning (Answer, pages 7 and 8), Swan discloses the claimed invention with the exception of the use of a random access memory (RAM) as a first memory element instead of a circulating shift register. To address this deficiency, the Examiner turns to the Springer reference which discloses the use of a random access memory (RAM) as a high-speed shift register. In the Examiner's view (Answer, page 8)

> It would have been obvious to one of ordinary skill in the DP art at the time of appellant's invention to incorporate Springer's RAM shift register into the Swan system, because Springer's RAM shift register would have increased the throughput of the Swan system by replacing slow-speed storage with high-speed RAM.

The Examiner, referring to Appellant's admissions at page 27, lines 11-17 of the specification, further asserts (Answer, page 14) the obviousness to the skilled artisan of placing the structure produced by

the combination of Swan and Springer on a single semiconductor chip to reduce circuit size.[3]

In response, Appellant initially asserts a lack of motivation for the Examiner's proposed combination of Swan and Springer. We do not agree. In our view, as asserted by the Examiner, Springer provides a clear suggestion to use high-speed RAM's in place of prior art slow-speed shift registers such as in Swan to increase data throughput.

We further find Appellant's argument as to lack of motivation for placing the combined structure of Swan and Springer on a single semiconductor chip to be unpersuasive. The miniaturization of computer circuitry for economy of space has been the goal of circuit designers since the dawn of the digital age. All of the evidence of record, including Appellant's own admissions in the specification, establishes that incorporation of all computer circuitry on a single semiconductor chip using large scale integration (LSI) was well known at the time of filing of Appellant's application. Appellant's arguments at page 11 of the Reply Brief to the effect that, while putting "non-invention" circuitry such as non-RAM correlators on an IC chip was well known, the

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[3]Independent claim 40 recites in the preamble "Single chip semiconductor means for signal processing . . . " while independent claim 1 recites only that "said first memory means is on a first single semiconductor chip."

placing of "invention" circuitry (unstated, but presumably the inclusion of a RAM memory) on a single chip was not well known, strains credulity. After weighing the totality of evidence, we remain overwhelmingly convinced of the obviousness to the skilled artisan of incorporating all of the elements recited in independent claims 1 and 40 on a single semiconductor chip. Accordingly, the Examiner's 35 U.S.C. § 103 rejection of independent claims 1 and 40 is sustained.

We note that Appellants' Briefs provide arguments for separate patentabiity of most of the dependent claims. We will consider these claims separately only to the extent separate arguments are of record in this appeal. Dependent claims 2, 3, 6, 15, 16, 18, 21, 24, and 27 have not been separately argued by Appellant and, accordingly, will be treated as standing or falling with their parent claims. See In re Young, 927 F.2d 588, 590, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991) ; In re Nielson, 816 F.2d 1567, 1572, 2 USPQ2d 1525, 1528 (Fed. Cir. 1987) and In re Wood, 582 F.2d 638, 642, 199 USPQ 137, 140 (CCPA 1978).

Dependent claims 4, 5, 7, and 8 are directed to various numbers of input and output lines as well as to parallel and serial operation. We do not dispute Appellant's arguments that the applied references do not explicitly disclose the claimed serial/parallel and input/output line combinations of these claims.

However, Appellant's minimal arguments do not address the issue of obviousness with respect to these claims. We are convinced, from the level of skill in this particular art, that the skilled artisan would have found it obvious to provide either parallel or serial operation with attendant design of appropriate numbers of input/output lines to accommodate the desired serial/parallel operations.

Further, Swan, at column 6, lines 1-18 discloses the second DELTIC memory circuit of claim 10, and, as combined with Springer, the first DELTIC RAM of claim 9. In addition, with respect to the digital delay line limitations of claim 26, Swan discloses at column 7, lines 1-31 a recirculating memory delay line which operates on digital signals. With regard to claims 11 and 12, Swan (column 2, line 72), when combined with Springer, discloses a first memory (e.g. registers 3 or 4) for shifting signals from location-to-location) and a second memory (from Springer) where signals are stationary.

We also note that the plural multiplier channels 170-176 of Swan describe the "set of multipliers" limitation of claim 17. Further, with respect to dependent claim 14, it is our view that the skilled artisan would have recognized the description of the logic operations at column 18, line 65-74 of Swan as the equivalent of an exclusive-OR operation.

We further find Appellant's arguments with respect to the control means limitations of claims 19 and 20 to be unpersuasive. Appellant argues that, contrary to the limitations of claim 19, Swan teaches the reading and writing of only a non-RAM memory at different rates while Springer teaches reading and writing at the same rate. Similarly, with regard to claim 20, Appellant contends that the address counter and clock in Swan shift signals only in a non-RAM memory while Springer's RAM does not shift signals. However, these references were used by the Examiner in combination to establish the basis for the obviousness rejection. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. In re Keller, 642 F.2d 413, 425, 208 USPQ 871, 881 (CCPA 1981); In re Merck & Co., Inc., 800 F.2d 1091, 1097, 231 USPQ 375, 380 (Fed. Cir. 1986)

Appellant's arguments with regard to the general purpose computer limitations of claims 22, 23, and 25 mirror those made with regard to the serial/parallel operations of claims 4, 5, 7, and 8. We do not dispute Appellant's arguments that neither Swan nor Springer explicitly discloses system control by a general purpose computer. We reiterate, however, that such minimal arguments do not address the issue of obviousness. In our view, the skilled artisan would clearly recognize the programmable advantages of a general purpose computer and, according-

ly, would have found it obvious to implement the combined system of Swan and Springer in general purpose computer form.

For all of the reasons discussed supra, it is our opinion that the Examiner has established a prima facie case of obviousness which remains unrebutted by any convincing arguments from Appellant. Accordingly, the Examiner's 35 U.S.C. § 103 rejection of independent claims 1 and 40, and claims -12 and 14-27 dependent thereon, is sustained.

In summary, with respect to appealed claims 1-12, 14-27, and 40, we have not sustained the Examiner's 35 U.S.C. § 112, first paragraph rejection, but have sustained the obviousness rejection under 35 U.S.C. § 103. Therefore, the decision of the Examiner rejecting claims 1-12, 14-27, and 40 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

"s/KENNETH W. HAIRSTON"
Administrative Patent Judge

"s/ERROL A. KRASS"
Administrative Patent Judge

"s/JOSEPH F. RUGGIERO"
Administrative Patent Judge

BOARD OF PATENT APPEALS AND INTERFERENCES

JFR:hh

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 23

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

MAILED
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BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JAMES N. CONSTANT

Appeal No. 1997—0239
Application No. 08/210,241

ON BRIEF

Before HAIRSTON, KRASS, and RUGGIERO, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

ON REQUEST FOR REHEARING

Appellant requests that we reconsider that portion of our decision of August 18, 2000 wherein we sustained the Examiner's rejection of claims 1—12, 14—27, and 40 under 35 U.S.C. § 103.

In our previous decision, we determined that the Examiner, based on the combination of the Swan and the Springer references, had established a prima facie case of obviousness which had not been persuasively rebutted by convincing arguments of Appellant. In particular, we found that the Examiner's line of reasoning established proper motivation to the skilled artisan to not only utilize the high speed RAM taught by Springer in place of the slower shift registers of Swan, but also to implement the combined circuitry of Swan and Springer on a single semiconductor chip.

Appellant has set forth several arguments alleging error in our original decision which sustained the Examiner's obviousness rejection. However, on reconsideration of our decision of August 18, 2000 in light of Appellant's comments in the Request for Rehearing, we find no error therein. We, therefore, decline to make any changes in our prior decision for the reasons which follow.

Appellant's initial argument relates to a procedural matter in which it is asserted that, since the

Swan and Springer references were before the Examiner during prosecution of Appellant's prior parent application which had a substantially identical disclosure and similar claims and which matured into U.S. Patent No. 3,950,635, such references can not be used to support a new question of patentability. We find, however, that this argument of Appellant is totally misplaced. The issue of "a substantial new question of patentability" as related to prior art cited during prosecution of an application which resulted in an issued patent arises in reexamination proceedings. Such issue is not relevant to the present appeal which does not involve a reexamination proceeding but, rather, an appeal of the Examiner's rejection in the latest of a series of continuation applications based on a continuation-in-part of the application which resulted in Appellant's Patent No. 3,950,635. See In re Hiniker Co., 150 F.3d 1362, 1367, 47 USPQ2d 1523, 1527 (Fed. Cir. 1998) cited by Appellant in the Request for Rehearing.

As to the merits of the Examiner's obviousness rejection, Appellant asserts a lack of explanation in the original Board decision of factors such as the understanding of the nature of the problem to be solved and the teachings in the applied references which would suggest the proposed combination. We find no error, however, in our initial finding of the obviousness to the skilled artisan of modifying the digital correlator of Swan by utilizing the high—

speed RAM of Springer, nor in our reasoning which led us to this conclusion. In our view, Springer discloses a clear recognition of the problem of achieving high—speed serial storage of data and the clear motivating suggestion to use a sequentially accessed RAM in place of slow-speed shift registers as in Swan.

Similarly, we find no error in our original finding of the obviousness to the skilled artisan of placing the combined structure of Swan and Springer on a single semiconductor chip. As we discussed in our original decision, the Examiner's line of reasoning sets forth a recognition of the circuit designer's goal of reducing circuit size as well as suggesting the motivation to the skilled artisan to use large scale integration techniques (LSI), which by Appellant's own admissions were available at the time of filing of the present application, to integrate all circuit elements into a single semiconductor chip.

We further point out that, contrary to Appellant's assertions at page 3 of the Request for Rehearing, admissions in Appellant's specification as to the prior art are valid as evidence to be considered in determining the issue of obviousness. In addition to Appellant's statement at page 27, lines 4-17 of the specification relating to prior art knowledge of large scale integration techniques, we point out the following statements by Appellant made during the course of prosecution of this application. At

page 16 of the amendment filed October 19, 1993, Appellant states "LSI puts all elements on a single semiconductor chip as disclosed in the references to Whitehouse and Byram, Buie and Brewer in the application, and as disclosed in parent Patent No. 3,950,635 (col. 2[,] lines 8—11, col. 6[,] lines 34—37, col. 7[,] lines 33—36)." Further, at page 8 of the amendment filed March 18, 1994, Appellant states "... putting circuits on a single semiconductor, ... are old art and need not be expressly detailed since these are known to one of ordinary skill."

We remain convinced for the reasons expressed in our original decision that the skilled artisan would have been motivated and would have found it obvious to modify the teachings of Swan by utilizing the high-speed RAM taught by Springer. In addition, we did not find, and do not find in this Request for Rehearing, any persuasive arguments presented by Appellant which would convince us that the skilled artisan, using well known large scale integration techniques, would not have found it obvious to implement the combined structural elements of Swan and Springer on a single semiconductor chip.

We have granted Appellant's request to the extent that we have reconsidered our decision of August 18, 2000, but we deny the request with respect to making any changes therein.

REHEARING/DENIED

"s/Kenneth W. Hairston"
Administrative Patent Judge

"s/Errol A. Krass
Administrative Patent Judge

BOARD OF PATENT
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"s/Joseph F. Ruggiero"
Administrative Patent Judge

JFR: tdl